REMARKS

Claims 1-4, 6-10, and 12-26 are pending. Claims 27-37 are being added. No new matter is being added.

This case was on appeal for the second time. The Fourth Non Final Office Action has reopened prosecution and has set forth new grounds of rejection.

Although the Office Action Summary page of the Fourth Non Final Office Action states that claim 15 stands rejected, the Fourth Non Final Office Action does not set forth a rejection for this claim. This claim was allowed as of the Second Appeal. Accordingly, Applicants will assume that this claim is allowed and will not discuss its patentablity over the cited art.

Prior Status of Case

This Office Action represents the Fourth Non Final Office Action for this case. No RCE or other types of continuations have been filed. In addition, there have been two Final Office Actions and two Appeal Briefs submitted. This represents the second time that the case has been with drawn from appeal.

Prior Art Rejections

Claims 1-4, 6-10, 12-14, 16-18, and 21-26 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitted Prior Art (AAPA) in view of Okuno, U.S. Patent No. 6,105,114 (Okuno). Claims 19-20 stand rejected over AAPA, Okuno, and further in view of Microsoft Press Computer Dictionary, Third Edition (MPCD).

Claims 1-2, 6-8, 12-14, 16, and 21-26 stand rejected under 35 U.S.C. 103(a) being unpatentable over Okuno and Ma et al, US Patent NO. 5,933,368 (Ma). Claims 3-4, 9-10, and 19-20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno and Ma and further in view of MPCD and AAPA.

These rejections are traversed for at least the reasons set forth below.

Independent Claim 1

a. No motivation to combine Okuno with Ma.

Claim 1 is allowable over Okuno and Ma under 35 U.S.C. 103(a) in that one of ordinary skill in the art would not be motivated to combine the teachings of Okuno and Ma.

Page 7 of the Fourth Non Final Office Action states that with regards to claim 1, Okuno teaches a memory but does not specifically state that it is a non volatile memory. Page 7 of the Fourth Non Final Office Action states that Ma discloses a non-volatile floating gate memory in column 1, lines 20-40 of Ma. Referring to that location of Ma, Ma discloses a flash memory.

Applicants respectfully submit that one of ordinary skill in the art would not be motivated to modify the circuit of Okuno to include the non volatile memory of Ma. Such a combination would render the circuit of Okuno inoperable for its intended purpose.

Okuno discloses a circuit for performing a transposition function on data. Specifically, Okuno discloses using a transposition memory circuit 1 for performing two-dimensional array transposition of blocks of NxN pixel data to implement a two dimensional discrete cosine transform (DCT). Okuno, column 1, lines 8-25, column 4, lines 5-9, and column 7, lines 31-47. Circuit 1 of Okuno includes a memory cell array 2 in which data can be written to and read from simultaneously and independent of each other. Okuno, column 5, lines 25-27 and column 10, lines 1-6. Accordingly, when the reading of data (e.g. one pixel) from a cell for a first block of data (of NxN pixel data) is complete, data from a next block of data can be written to the cell. See Okuno, column 9, line 51 to column 10, line 16 where it describes how data from a first block (data that was previously written) is read from the memory cells of array 2 while data from a second block is written to the memory cells of array 2. See also Okuno, column 10, lines 17 to column 10, line 34 where it describes how data from the second block is read from the memory cells of array 2 while data from a third block is written to the memory cells. See also column 6, lines 27-44 stating how data is processed by successively reading in and writing out data in a different direction. For accomplishing these operations, memory cell array 2 is responsive to a

clock signal for writing data to a memory cell at a rising edge of a clock signal and reading data from a memory cell at a falling edge of a clock signal. Okuno, column 7, lines 48-66.

The ability to perform the operations above enables circuit 1 to perform the transportations of a two dimension array of data with one memory cell array and without using two memory cell arrays. Okuno column 4, lines 32-40; column 5, lines 5-12; column 5, lines 40-42; column 6, lines 6-9 and lines 50-52; and column 11, lines 27-35. The ability to perform these operations without two memory arrays is enabled by the use of a memory array having memory cells that can be written to and read from simultaneously. See Okuno, Column 5, lines 25-27 and lines 44-46; column 6, lines 10-14 and lines 51-54; column 8, lines 37-40; and column 10, lines 1-6. The ability of circuit 1 of Okuno to perform the desired operations without two memory arrays results in reducing circuit scale and power consumption. Okuno, column 4, lines 38-40; column 5, lines 12-14; column 6, lines 21-23 and lines 56-58; and column 11, lines 31-36. Also, such a memory array enables the circuit to have the same processing speed as conventional circuitry. See Okuno, column 5, lines 47-49; column 6, lines 14-15 and lines 24-26, and column 6, lines 54-56.

One of ordinary skill in the art would not be motivated to include the nonvolatile memory taught in Ma in the circuit of Okuno because Ma does not teach that its memory array can be written to and read from simultaneously and independently of each other.

Ma discloses a nonvolatile memory such as a flash memory. Ma, column 1, lines 6 to column 2, line 25. Ma does not disclose that its nonvolatile memory is a cell array in which data can be written to and read from simultaneously and independently of each other. In fact, Ma specifically teaches that with flash memory, existing data cannot be directly over written with new data. Ma teaches that with flash memory, the memory needs to be erased first so that it becomes "clean" before new data can be written. Ma teaches that in contrast, other types of RAM can be over written with new data. Ma, column 3, lines 28-44. Thus, the non volatile flash memory of Ma could not be utilized in the circuit Okuno in that data could not be written to and read from simultaneously.

Furthermore, Ma teaches that to erase flash memory, a high voltage needs to be applied to the cells of the terminals. In addition, to erase a flash memory, "the entire memory (or some

sub-portions thereof) needs to be erased at the same time." Ma specifically teaches that this is different from other RAM in which individual bits can be erased and written. Ma, column 1, lines 49-57. This mass erase requirement of flash memory as taught by Ma makes flash unusable in the circuit of Okuno in that Okuno requires that a specific cell be written after the cell has been read and that the next cell be read after the write. Okuno, column 6, lines 27 to 44 and column 10 lines 4-7. The mass erase feature would mean that a subsequent read of an adjacent cell could not be made, and the flash memory could not perform the transposition function.

Accordingly, one of skill in the art could not implement circuit 1 of Okuno with the flash memory of Ma in that the flash memory of Ma can not be written to and read from simultaneously for successive read-writes in that Ma would require an erase operation before data could be read. Thus, memory circuit 1 of Okuno modified to include the flash memory of Ma could not perform the transposition operations as set forth in Okuno. See MPEP Section 2143.01, Subsection THE PROPOSED MODIFICATION CANNOT RENDER THE PRIOR ART UNSATISFACTORY FOR ITS INTENDED PURPOSE and the subsection entitled THE PROPOSED MODIFICATION CANNOT CHANGE THE PRINCIPLE OF OPERATION OF A REFERENCE.

Furthermore, as set forth above, Okuno teaches a desirability for processing speed. Ma on the other hand explicitly teaches that its flash memory is slower than compared to other types of memory. Ma, column 1, lines 58-64. Accordingly, one of skill in the art would not be motivated to modify circuit 1 of Okuno with the flash memory of Ma in that it would decrease operating speed.

Furthermore, Okuno explicitly teaches away from the use of a memory like that set forth in Ma. Okuno explicitly teaches that its objective is to reduce power consumption, and more specifically, reduce power by lowering "the supply voltage or the like." Okuno, column 3, lines 60-64. However, Ma teaches that a high erase voltage is needed for erasing a flash memory. Ma, column 1, lines 49-50. Accordingly, one of skill in the art would be not be motivated to use the flash memory of Ma in the circuit of Okuno in that the memory array of Ma requires a high voltage for writing and that Okuno specifically teaches against using a high voltage.

As set forth above, Okuno also teaches the desirability to reduce circuit scale. However, implementing the nonvolatile memory of Ma in circuit 1 of Okuno would require that circuit 1 of Okuno include high voltage generation and erase circuitry to erase a flash memory. Accordingly, one of skill in the art would not be motivated to modify the circuit of Okuno to include the flash memory of Ma in that it would require that circuit 1 of Okuno have extra circuitry (including extra circuitry operating at higher voltages), which is explicitly taught away from in Okuno.

In addition, because the system of Okuno requires multiple reads and writes of the same cells for processing data, one of skill in the art would not be motivated to include a flash memory as taught in Ma due to the limited number of lifetime erase-write cycles of such memories. See Ma, column 1, lines 31-48.

Page 7 of the Fourth Non Final Office Action sets forth a motivation combine Okuno with Ma. Specifically, page 7 of the Fourth Non Final Office Action states:

> it would have been obvious to one of ordinary skill .... having the teachings of Okuno and Ma et al before him/her, to use a non-volatile memory as the memory in the system of Okuno, because it is light in weight, occupies very little space, and consumes less power, as discussed in column 1, lines 26-27 of Ma et al.

Applicants respectfully submit that this is not a proper motivation to combine the flash memory of Ma in the circuit of Okuno. The above advantages stated in Ma are advantages of a flash memory over other types of non volatile memory such as hard disks. See Ma, column 1, lines 13-30. Ma does not state these are advantages of a flash memory over the type of a RAM used in Okuno. In fact, Ma specifically states that flash memory has several disadvantages over a RAM that is used in Okuno such that it has a finite number of erase/write cycles as compared to RAM (column 1, lines 31-48), that it requires a high erase voltage (Ma, column 1, lines 49-53), that individual bits can not be erased and written like RAM (Ma, column 1, 54-56), and that it is slower (Ma, column 1, lines 58-64). Accordingly, such advantages of flash memory identified by the Fourth Non Final Office Action would not be advantages in using a flash memory like Ma to replace the RAM array in the circuit of Okuno.

Accordingly, claim 1 is allowable over Okuno and Ma.

b. no motivation to combine Okuno with AAPA

Pages 3-4 of the Fourth Non Final Office Action state that claim 1 is obvious under 35 U.S.C. 103(a) over AAPA in view of Okuno. Page 4 of the Fourth Non Final Office Action states that the difference between AAPA and the claims is the explicit recitation of a bit of the second portion being more significant that a bit of the first portion. However, page 4 of the Fourth Non Final Office Action states that Okuno discloses "just such an address transposition."

Page 4 of the Fourth Non Final Office Action specifically states that it would have been obvious "to modify the prior art system of AAPA to transpose the addresses (thereby switching the most and least significant bits of the address) as in Okuno, because it will reduce circuit scale as well as power consumption, as discussed in Okuno at column 4, lines 7-9."

Applicants respectfully submit that the above is not a proper motivation to combine the teachings of AAPA with Okuno. Applicants respectfully submit that adding the transposing addresses feature of Okuno to the memory system of AAPA will not reduce circuit scale and power consumption.

Okuno discloses a system for performing a transposition function on data. Specifically, Okuno discloses using a transposition memory circuit 1 for performing two-dimensional array transposition of blocks of NxN pixel data to implement a two dimensional discrete cosine transform (DCT). Okuno, column 1, lines 8-25, column 4, lines 5-9, and column 7, lines 31-47.

When Okuno states that its circuit provides for reduced circuit scale and power consumption, its circuit obtains these advantages over conventional circuits that perform the transposition function. See for example column 3, line 65 to column 4, line 2 of Okuno where it describes that conventional transposition memory circuit 101 includes two cell arrays for performing transposition functions. See also column 4, lines 36-40 of Okuno where it states that because its transposition circuit can perform transposition functions by using one, two-dimensional array instead of two arrays, circuit scale can be reduced to decrease power consumption over a conventional transposition circuit. Accordingly, these advantages of reduced circuit scale and power consumption as set forth in Okuno are achieved only with respect to other conventional circuits that perform transposition functions.

Because the circuit of AAPA does not perform the function of transposing data, there is no teaching, reason, or suggestion to one of skill in the art that modifying the non volatile memory of AAPA as per the teaching of Okuno would obtain the benefits of decreased circuit scale and power consumption.

Furthermore, nowhere in the disclosure of Okuno does it state, suggest, imply, or even hint that its teachings can be applied to save power and reduce circuitry scale in non volatile memory systems with floating gate type cells such as that of AAPA.

In fact, implementing the address transposing function of Okuno in the memory of AAPA would actually require additional circuitry (and consume more power) than the unmodified memory system of AAPA. To implement the address transposing function of Okuno in AAPA, an address translation circuit 5 (see Figure 12 of Okuno) and SEL signal generation circuit (see Figure 13 of Okuno) would have to be added to the memory system of AAPA. Column 10, line 45 to column 11, line 24 of Okuno describes how the address translation circuit can switch address lines between column and row decoder inputs (Okuno, column 10, lines 50-67). This additional circuitry, as well as the SEL generation circuit of Figure 13 of Okuno, would increase circuit scale and power consumption in the memory system of AAPA, not reduce it.

Although the ability to transpose addresses may allow for a reduction in the number of memory arrays to be used in a conventional circuit for performing transposition functions, such reduction in array circuitry would not be achieved in the memory system of AAPA by adopting the transposing address function of Okuno. In fact, the addition of such a feature in the memory of AAPA would act to increase circuit scale and power. Accordingly, one of skill in the art would not be motivated to add the address transporting function of Okuno to the memory of AAPA.

c. AAPA and Okuno are not analogous art.

It is improper to combine the Okuno reference and AAPA in that the Okuno reference is not analogous art to the non volatile memory system as taught in AAPA.

AAPA discloses a memory system having a non volatile memory and circuitry for accessing cells of the memory.

Okuno, on the other hand, discloses a specialized circuit for performing a transposition function on data. Specifically, Okuno discloses using a memory circuit 1 for performing two-dimensional array transposition of blocks of NxN pixel data to implement a two dimensional discrete cosine transform (DCT). Okuno, column 1, lines 8-25, column 4, lines 5-9, and column 7, lines 31-47.

One of skill in the art would not look to the teachings of Okuno to modify the non volatile memory system of AAPA in that Okuno is a reference describing a specialized circuit for performing a transposition function. The circuit of Okuno uses a two-dimensional array having particular characteristics for performing that function. Okuno requires an array to perform specific functions that the non volatile memory of AAPA can not perform (see the above discussion of Ma regarding the limitations of a flash memory). Thus, one of skill in the art would not look to the teachings of Okuno to modify the non volatile memory of AAPA.

Accordingly, Okuno is not in the field of endeavor of AAPA, nor is it pertinent to the problem set forth in AAPA (reducing read disturb in a non volatile memory). See page 2, lines 3-9 of the specification of the present application.

Furthermore, just because Okuno and AAPA describe memory circuits, that alone does not mean that they are in the same field of endeavor. Applicants respectfully direct the Examiner to MPEP section 2141.01(a), subsection entitled ANOLOGY IN THE ELECTRICAL ARTS. This subsection cites Wang v. Toshiba, 26 USPQ2d 1767 (Fed. Cir. 1993). This case stands for the proposition that just because the claims and prior art were both directed to single in-line memory modules (SIMM), that alone did not mean that the claims and art were in the same field of endeavor.

Accordingly, claims Okuno and AAPA are not analogous art and their combination for an obviousness rejection under 35 U.S.C. 103(a) is improper.

Because the Fourth Non Final Office Action has not set forth a prima facie motivation to combine AAPA with Okuno and because AAPA and Okuno are not analogous art, claim 1 is allowable over AAPA and Okuno.

Independent Claims 6, 14, 16, 22, and 25

Independent claims 6, 14, 16, 22, and 25 stand rejected under 35 U.S.C. 103(a) over Okuno in view of Ma and over AAPA in view of Okuno.

For reasons similar to those stated above with respect to independent claim 1, these claims are allowable over Okuno and Ma and over AAPA and Okuno in that the Fourth Non Final Office Action has not set forth prima facie motivations to combine Okuno and Ma and AAPA and Okuno, and because Okuno and AAPA are non analogous art. Accordingly, these independent claims are allowable.

Dependent Claims

Each dependent claim depends from an independent claim and is allowable for at least this reason.

The application is believed to be in condition for allowance and notice of such is respectfully requested. If there is any remaining issues, the Examiner is respectfully requested to telephone the undersigned.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079.

Respectfully submitted,

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.
Law Department

Customer Number: 23125

By: /David G. Dolezal/
David G. Dolezal
Attorney of Record
Reg. No.: 41,711
Telephone: (512) 996-6839
Fax No.: (512) 996-6854